PIC16F73/74/76/77

PIC16F73/74/76/77 Rev. B1 Silicon/Data Sheet Errata

The PIC16F73/74/76/77 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS30325**B**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16F73/74/76/77 silicon.

1. Module: Timer1

When Timer1 is running in Asynchronous mode and then disabled, data in the Timer1 register (TMR1) may become corrupted. Corruption occurs when the timer enable is turned off at the same instant that a ripple carry occurs in the timer module.

This issue only occurs in asynchronous operation. In synchronous operation, the relevant signals are latched with the CPU clock and the problem condition does not arise.

Revision C silicon will correct this issue.

Work around

When Timer1 is configured to operate as an asynchronous counter, care must be taken that there is no incoming pulse while the module is being turned off. If an incoming pulse arrives while Timer1 is being turned off, the value of register TMR1 may become corrupted.

If an application requires that Timer1 be turned off, and if it is possible that Timer1 may receive an incoming pulse while being turned off, synchronize the external clock first by clearing the T1SYNC bit of register T1CON (T1CON<2>). Please note, however, that this may cause Timer1 to miss up to one count.

Date Codes that pertain to this issue:

PIC16F73/74	0219 and earlier
PIC16F76/77	0303 and earlier

2. Module: CCP (Compare Mode)

The output of the CCP module in Compare mode may become inverted when the mode of the module is changed from Compare/Clear on Match (CCPxM<3:0> = `1001`) to Compare/Set on Match (CCPxM<3:0> = `1000`). This may occur as a result of any operation that selectively clears bit CCPxM0, such as a `BCF` instruction.

When this condition occurs, the output becomes inverted when the instruction is executed. It will remain inverted for all following compare operations until the module is reset.

Revision C silicon will correct this issue.

Work around

Do not selectively clear bit CCPxM0 to select the Compare/Set on Match mode. Instead, clear the entire CCPxCON register, which resets the module. Follow this with an instruction to set CCPxM3 (CCPxCON<3>), which selects the Set on Match mode.

Date Codes that pertain to this issue:

PIC16F73/74	0219 and earlier
PIC16F76/77	0303 and earlier

3. Module: Oscillator (HS mode)

When resonators above 2 MHz are used, the HS mode oscillator is required to ensure reliable operation. HS mode oscillator drive at frequencies from 2 MHz to 4 MHz is often excessive, resulting in the amplitude of the oscillator waveform exceeding VDD and VSS. In such cases, the waveform may experience distortion as ESD protection devices begin to operate on the OSC1 and OSC2 pins. This distortion appears as a non-sinusoidal waveform or clipping, and can generate substantial harmonics that may create excessive noise in the application.

Revision C silicon will correct this issue.

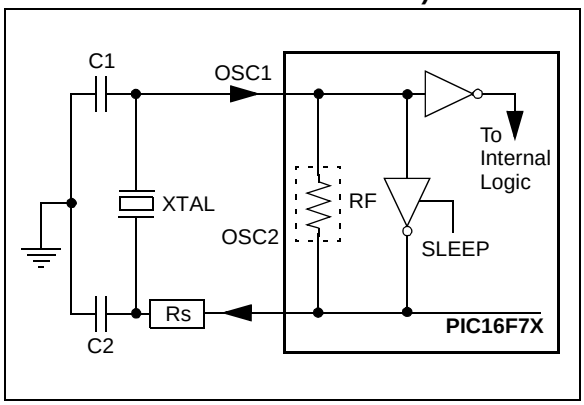
Work around

The gain of the oscillator should be reduced by inserting a series resistance between the OSC2 pin and the resonator/capacitor as shown in the data sheet (see Figure 1). The value of the series resistance is dependant on VDD, resonator frequency, and temperature; however, 330 ohms has been used as a good starting point for evaluation.

This change will not affect operation of future revisions of silicon as long as HS mode is selected.

Note:	This issue applies only to resonators above 2 MHz in Revision B silicon. No issues are known to exist with crystals at any frequency using XT Oscillator mode.

FIGURE 1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Date Codes that pertain to this issue:

PIC16F73/74	0219 and earlier
PIC16F76/77	0303 and earlier

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30325**B**), the following clarifications and corrections should be noted.

1. Module: Core

The typical and maximum supply currents (parameter D010A) specified for extended voltage devices have been changed.

The IDD specifications differ from the Device Data Sheet only for devices operating at a VDD of 3.0V and a FOSC of 32 kHz with the WDT disabled.

The changes in the specification are shown in **bold** in Table 1.

Work around

None.

Date Codes that pertain to this issue:

All.

TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic/ Device	New Specification			Data Sheet Specification			Units	Notes
			Min	Typ	Max	Min	Typ	Max		
D010A	IDD	**Supply Current** PIC16LF73/74/76/77	—	**25**	48	—	20	48	µA	LP osc configuration, FOSC = 32 kHz, VDD = 3.0V, WDT disabled

2. Module: Pinout Correction

The MLF (now known as QFN) package pinout locations for pins RA4 and RA5 were incorrectly stated in Table 1-2 of the Device Data Sheet.

The correct pinout locations are indicated in **bold** in Table 2.

TABLE 2: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
.					
.					
.					
RA4/T0CKI	6	**3**		ST	
RA4			I/O		Digital I/O – Open drain when configured as output.
T0CKI			I		Timer0 external clock input.
RA5/$\overline{SS}$/AN4	7	**4**		TTL	
RA5			I/O		Digital I/O.
$\overline{SS}$			I		SPI slave select input.
AN4			I		Analog input 4.
.					
.					
.					

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

3. Module: Pinout Correction

The PIC16F73/74/76/77 device family does not offer low-voltage programming. The Device Data Sheet incorrectly lists RB3 as providing the PGM function required for low-voltage programming.

References to the PGM function in Tables 1-2 and Table 1-3 of the Device Data Sheet have been removed. Table 3 and Table 4 show the corrections for the PIC16F73/76 and PIC16F74/77 devices respectively, The text shown in ~~**bold**~~ has been removed.

References to the PGM function in the Pin Diagrams on pages 2 and 3, and Figures 1-1 and 1-2 (pages 6 and 7) in the Data Sheet have also been removed.

A reference to the PGM function listed in the Data Sheet Index has also been removed.

TABLE 3: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
.					
.					
.					
RB3~~/PGM~~	24	21		TTL	
RB3			I/O		Digital I/O.
~~PGM~~			~~I/O~~		~~Low-voltage ICSP programming enable pin.~~
.					
.					
.					

TABLE 4: PIC16F74 AND PIC16F77 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
.						
.						
.						
RB3~~/PGM~~	36	39	11		TTL	
RB3				I/O		Digital I/O.
~~PGM~~				~~I/O~~		~~Low-voltage ICSP programming enable pin.~~
.						
.						
.						

4. Module: Packaging (Pinout and Product Identification)

PIC16F74 and PIC16F77 devices are now offered in a 44-pin, micro lead frame package (commonly known as “QFN”). This provides near chip scale package size. This option is in addition to the 28-pin QFN packages already available for the PIC16F73 and PIC16F76 devices. The 44-pin QFN package has been added to the product line since the original publication of the Device Data Sheet.

The addition of this option requires the following additions to the Device Data Sheet (DS30325**B**). Referenced figures and tables follow this text.

1. The “Pin Diagrams” on pages 2-3 of the Data Sheet are amended with the addition of the 44-pin QFN pinout shown in Figure 2.
2. Table 1.3 of Section 1.0 (“Device Overview”) is replaced with an updated version which adds a column for QFN pin assignments. All new information is indicated in **bold**.
3. Section 17.1 (“Package Marking Information”) is amended to include a marking template and example for 44-pin QFN devices. These are shown in Figure 3.
4. Section 17.2 (“Package Details”) is amended to include the mechanical drawing of the 44-pin QFN package, following the existing drawings. This is shown in Figure 4.
5. In the “PIC16F7X Product Identification System” (page 171), the “ML” line item in the “Package” options section should now read (change in **bold**):

   ML = **QFN**

   For the sake of completeness, it is also noted that the package designation “MLF” is now replaced by “QFN” in all occurrences throughout the Device Data Sheet. “MLF” should be considered an obsoleted term.

FIGURE 2: PINOUT DIAGRAM FOR PIC16F74/77, 44-PIN QFN PACKAGE

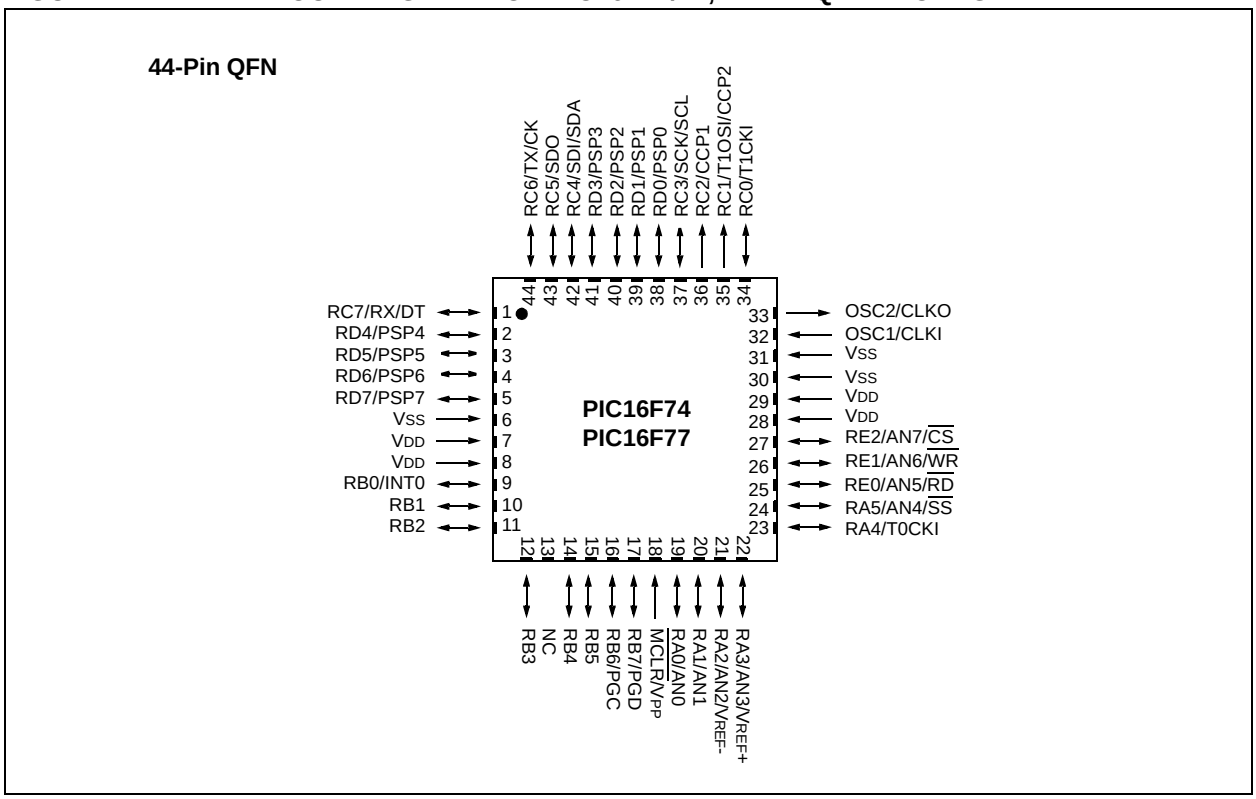


FIGURE 3: PACKAGE MARKING TEMPLATE FOR PIC16F74/77, 44-PIN QFN

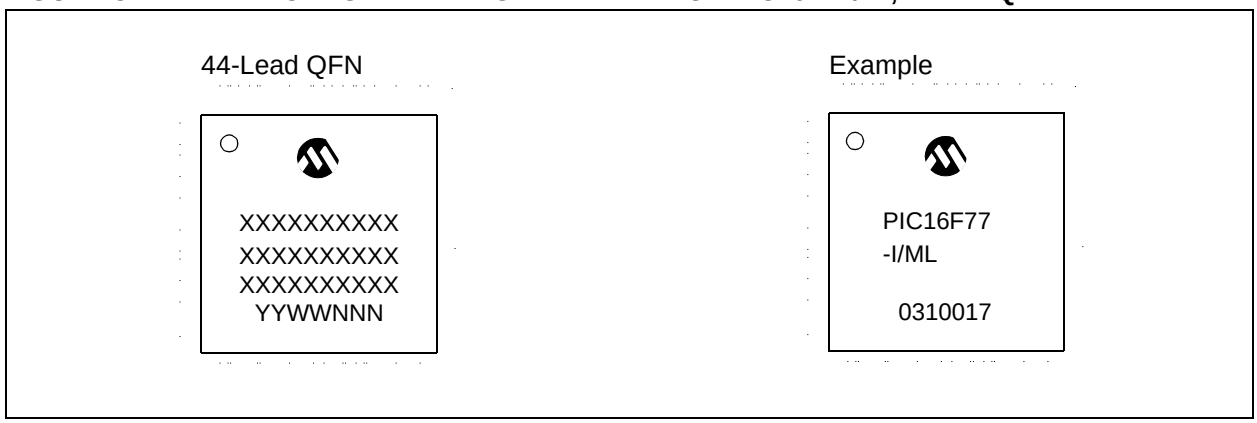


TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI	13	14	**32**	30	I	ST/CMOS(4)	Oscillator crystal or external clock input.
OSC1							Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
CLKI							External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	14	15	**33**	31	O	—	Oscillator crystal or clock output.
OSC2							Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO							In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	**18**	18	I/P	ST	Master Clear (input) or programming voltage (output).
$\overline{MCLR}$							Master Clear (Reset) input. This pin is an active low RESET to the device.
VPP							Programming voltage input.
							PORTA is a bidirectional I/O port.
RA0/AN0	2	3	**19**	19		TTL	
RA0					I/O		Digital I/O.
AN0					I		Analog input 0.
RA1/AN1	3	4	**20**	20		TTL	
RA1					I/O		Digital I/O.
AN1					I		Analog input 1.
RA2/AN2/VREF-	4	5	**21**	21		TTL	
RA2					I/O		Digital I/O.
AN2					I		Analog input 2.
VREF-					I		A/D reference voltage (Low) input.
RA3/AN3/VREF+	5	6	**22**	22		TTL	
RA3					I/O		Digital I/O.
AN3					I		Analog input 3.
VREF+					I		A/D reference voltage (High) input.
RA4/T0CKI	6	7	**23**	23		ST	
RA4					I/O		Digital I/O – Open drain when configured as output.
T0CKI					I		Timer0 external clock input.
RA5/$\overline{SS}$/AN4	7	8	**24**	24		TTL	
RA5					I/O		Digital I/O.
$\overline{SS}$					I		SPI slave select input.
AN4					I		Analog input 4.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
							PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	**9**	8		TTL/ST(1)	
RB0					I/O		Digital I/O.
INT					I		External interrupt.
RB1	34	37	**10**	9	I/O	TTL	Digital I/O.
RB2	35	38	**11**	10	I/O	TTL	Digital I/O.
RB3	36	39	**12**	11	I/O	TTL	Digital I/O.
RB4	37	41	**14**	14	I/O	TTL	Digital I/O.
RB5	38	42	**15**	15	I/O	TTL	Digital I/O.
RB6/PGC	39	43	**16**	16		TTL/ST(2)	
RB6					I/O		Digital I/O.
PGC					I/O		In-circuit debugger and ICSP™ programming clock.
RB7/PGD	40	44	**17**	17		TTL/ST(2)	
RB7					I/O		Digital I/O.
PGD					I/O		In-circuit debugger and ICSP™ programming data.
							PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	16	**34**	32		ST	
RC0					I/O		Digital I/O.
T1OSO					O		Timer1 oscillator output.
T1CKI					I		Timer1 external clock input.
RC1/T1OSI/CCP2	16	18	**35**	35		ST	
RC1					I/O		Digital I/O.
T1OSI					I		Timer1 oscillator input.
CCP2					I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	17	19	**36**	36		ST	
RC2					I/O		Digital I/O.
CCP1					I/O		Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	**37**	37		ST	
RC3					I/O		Digital I/O.
SCK					I/O		Synchronous serial clock input/output for SPI™ mode.
SCL					I/O		Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI/SDA	23	25	**42**	42		ST	
RC4					I/O		Digital I/O.
SDI					I		SPI data in.
SDA					I/O		I^2C data I/O.
RC5/SDO	24	26	**43**	43		ST	
RC5					I/O		Digital I/O.
SDO					O		SPI data out.
RC6/TX/CK	25	27	**44**	44		ST	
RC6					I/O		Digital I/O.
TX					O		USART asynchronous transmit.
CK					I/O		USART 1 synchronous clock.
RC7/RX/DT	26	29	**1**	1		ST	
RC7					I/O		Digital I/O.
RX					I		USART asynchronous receive.
DT					I/O		USART synchronous data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
							PORTD is a bidirectional I/O port or parallel slave port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	**38**	38		ST/TTL(3)	
RD0					I/O		Digital I/O.
PSP0					I/O		Parallel Slave Port data.
RD1/PSP1	20	22	**39**	39		ST/TTL(3)	
RD1					I/O		Digital I/O.
PSP1					I/O		Parallel Slave Port data.
RD2/PSP2	21	23	**40**	40		ST/TTL(3)	
RD2					I/O		Digital I/O.
PSP2					I/O		Parallel Slave Port data.
RD3/PSP3	22	24	**41**	41		ST/TTL(3)	
RD3					I/O		Digital I/O.
PSP3					I/O		Parallel Slave Port data.
RD4/PSP4	27	30	**2**	2		ST/TTL(3)	
RD4					I/O		Digital I/O.
PSP4					I/O		Parallel Slave Port data.
RD5/PSP5	28	31	**3**	3		ST/TTL(3)	
RD5					I/O		Digital I/O.
PSP5					I/O		Parallel Slave Port data.
RD6/PSP6	29	32	**4**	4		ST/TTL(3)	
RD6					I/O		Digital I/O.
PSP6					I/O		Parallel Slave Port data.
RD7/PSP7	30	33	**5**	5		ST/TTL(3)	
RD7					I/O		Digital I/O.
PSP7					I/O		Parallel Slave Port data.
							PORTE is a bidirectional I/O port.
RE0/$\overline{RD}$/AN5	8	9	**25**	25		ST/TTL(3)	
RE0					I/O		Digital I/O.
$\overline{RD}$					I		Read control for parallel slave port.
AN5					I		Analog input 5.
RE1/$\overline{WR}$/AN6	9	10	**26**	26		ST/TTL(3)	
RE1					I/O		Digital I/O.
$\overline{WR}$					I		Write control for parallel slave port.
AN6					I		Analog input 6.
RE2/$\overline{CS}$/AN7	10	11	**27**	27		ST/TTL(3)	
RE2					I/O		Digital I/O.
$\overline{CS}$					I		Chip select control for parallel slave port.
AN7					I		Analog input 7.
VSS	12,31	13,34	**6, 30, 31**	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	**7, 8, 28, 29**	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17, 28,40	**13**	12,13, 33,34	—	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

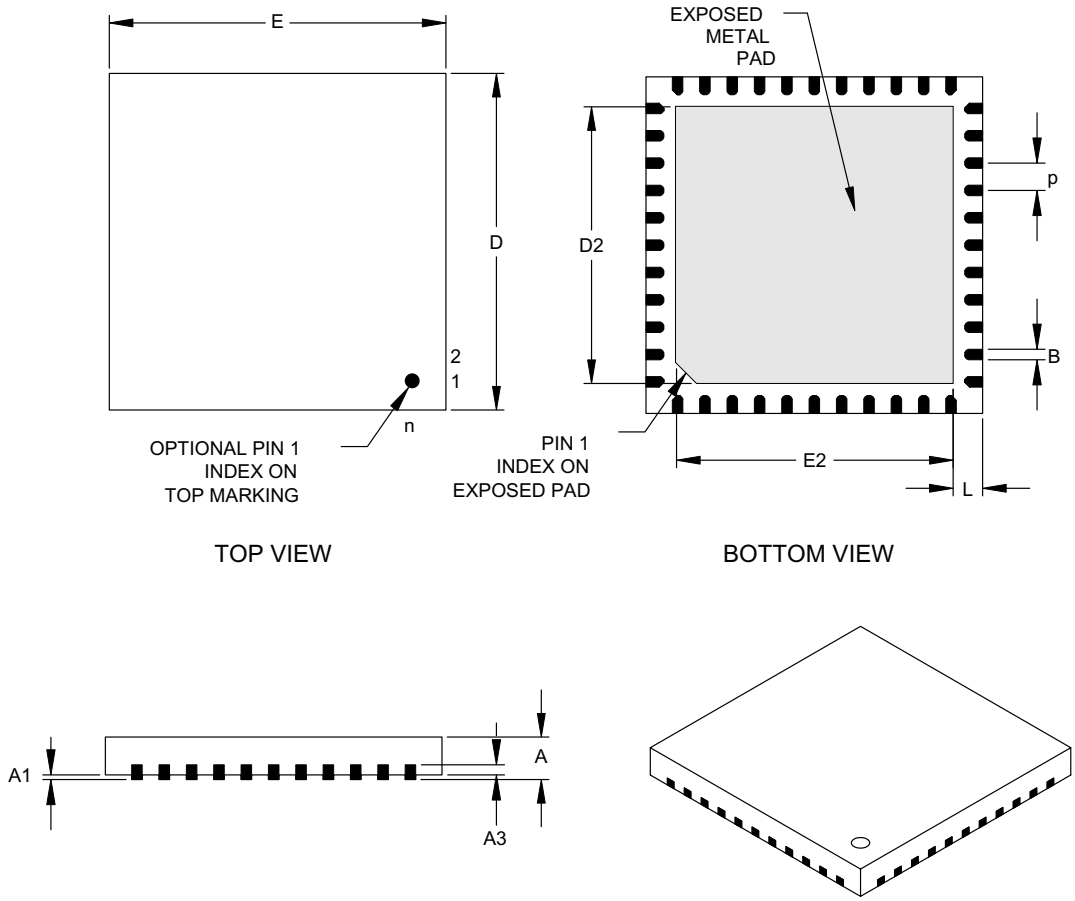
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

FIGURE 4: 44-PIN QFN PACKAGE (DRAWING 1, PACKAGING)

44-Lead Plastic Quad Flat No Lead Package (ML) 8x8 mm Body (QFN)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0	0.02	0.05
Base Thickness	A3		.010 REF			0.25 REF	
Overall Width	E		.315 BSC			8.00 BSC	
Exposed Pad Width	E2	.262	.268	.274	6.65	6.80	6.95
Overall Length	D		.315 BSC			8.00 BSC	
Exposed Pad Length	D2	.262	.268	.274	6.65	6.80	6.95
Lead Width	B	.012	.013	.013	0.30	0.33	0.35
Lead Length	L	.014	.016	.018	0.35	0.40	0.45

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: M0-220

Drawing No. C04-103

REVISION HISTORY

Rev A Document (2/01)

Original errata document for PIC16F77 (DS80099A). Issue 1 (Timer1), page 1.

Rev B Document (4/01)

Addition of other members of 16F7X family for issue 1. Added issue 2 (Core), page 1 and issue 3 (A/D), page 2.

Rev C Document (7/01)

Added issue 4 (CCP), page 2 and issue 5 (Core), page 3.

Rev D Document (8/01)

Under Clarifications/Corrections to the Data Sheet, added issue 1 (Reset), page 4.

Rev E Document (9/02)

Removed previous Clarifications/Corrections to the Data Sheet (DS30325A), added Issue 6 (Oscillator), page 4.

Rev F Document (1/03)

Removed previous silicon issue 2 (Core) and silicon issue 3 (A/D), updated silicon issue 1 (Timer1), silicon issue 2 (formerly issue 4, Compare Mode) and silicon issue 3 (formerly issue 6, HS Mode) with new date code information. Moved previous silicon issue 5 (Core) to Clarifications/Corrections to the Data Sheet (DS30325B) and added issue 2 (Pinout Correction).

Rev G Document (8/03)

Added Data Sheet Clarification issues 3 (Pinout Correction) and 4 (Packaging).

Note the following details of the code protection feature on Microchip devices:

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